This listing of claims replaces all prior versions, and listings of claims in the application:

LISTING OF THE CLAIMS

1. (currently amended) A process for controlling a multiple core expander comprising:

using a test port of said multiple core expander to receive both data values as well as instructional and operational codes including a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to said multiple core expander to put all but one core expander of said multiple core expander in bypass mode;

decoding ~~the~~ said instructional and operational input codes by a state machine of ~~the~~ said one core expander not placed in bypass mode;

serially reading data from, and serially writing data to, at least one internal register of said one core expander not placed in bypass mode by ~~the~~ said state machine;

~~the state machine inputting~~ transmitting a control signal from said state machine to a multiplexer to shift data to ~~the~~ an output port of ~~the~~ said one core expander not placed in bypass mode to either a series connected core expander or back to ~~the~~ said host computer; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said multiple core expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

2. (currently amended) A method of controlling ~~the~~ operation of a dual expander having a first expander core and a second expander core by reading and writing control bits through a single test port in said dual expander comprising:

placing one of said first expander core and said second expander core ~~in~~ into bypass mode utilizing a single bit shift register;

transmitting a serial data stream of said control bits as data values and instructional and operational codes through said test port to a shift register to generate a control byte for the expander core that is not in bypass mode;

parallel shifting said control byte from said shift register to a single bit shift register ~~in~~ into said one of said first expander core and said second expander core that is not in bypass mode;

providing dummy bits in said serial data stream to correctly form said control byte for ~~the~~ said one of said first expander core and said second expander core that is not in bypass mode; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said dual expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

3. (currently amended) A process for performing a register write operation in a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port, said operational code bits including data plus instructions with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to place ~~the~~ a second expander core, in said dual expander, ~~in~~ into bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core ~~in~~ into bypass mode in response to said operational byte;

serially shifting control data bits, address bits and write command bits of said operational control bits into said test port;

reading ~~the~~ said serially shifted control data bits, address bits and write command bits by a state machine;

generating a control byte by ~~the~~ said state machine from said control data bits and an address byte from said address bits;

writing said control byte by ~~the~~ said state machine to a register in said first expander core at an address indicated by said address byte; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said dual expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

4. (currently amended) A process for performing a register write operation in a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including data plus instructions with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to place the first expander core, in said dual expander, ~~in~~ into bypass mode utilizing a single bit shift register;

generating an operational byte from said operational code bits;

placing said first expander core ~~in~~ into bypass mode in response to said operational byte;

shifting control data bits, address bits and write command bits into said test port;

reading ~~the~~ said serially shifted control data bits, address bits and write command bits by a state machine;

generating a control byte by ~~the~~ said state machine from said control data bits and an address byte from said address bits;

writing said control byte by ~~the~~ said state machine to a register in said second expander core at an address indicated by said address byte; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said dual expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

5. (currently amended) A process for performing a register read operation from a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including data plus instructions with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to place the second expander, in said dual expander, ~~in~~ into bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core ~~in~~ into bypass mode in response to said operational byte;

serially shifting read address bits and a read command into said test port of said dual expander;

generating an address byte by a state machine from said read address bits;

serially reading data by ~~a~~ said state machine from a register in said first expander core at an address indicated by said address byte through said test port of said dual expander; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said dual expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

6. (currently amended) A process for performing a register read operation from a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including data plus instructions with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to place the first expander, in said dual expander, ~~in~~ into bypass mode;

generating an operational byte from said operational code bits;

placing said first expander core ~~in~~ into bypass mode in response to said operational byte;

serially shifting read address bits and a read command into a test port of said dual expander;

generating a read address byte by a state machine from said read address bits;

serially reading data by ~~a~~ said state machine from a register in said second expander core at an address indicated by said address byte through said test port of said dual expander; and

connecting internal registers to an expander bus wherein ~~the~~ said internal registers store data that is used to operate ~~the expanders for the performance of~~ said dual expander in order to perform various operations ~~such as adjusting the slew rate, delay time, etc~~.

7. (new) The process for controlling said multiple core expander of claim 1 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

8. (new) The method of controlling operation of said dual expander having said first expander core and said second expander core of claim 2 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

9. (new) The process for performing said register write operation in said first expander core of said dual expander of claim 3 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

10. (new) The process for performing said register write operation in said second expander core of said dual expander of claim 4 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

11. (new) The process for performing said register read operation from said first expander core of said dual expander of claim 5 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

12. (new) The process for performing said register read operation from said second expander core of said dual expander of claim 6 wherein said various operations comprise at least one of the group comprising: adjusting slew rate and adjusting delay time.

13. (new) The process for performing a register read operation from a first expander core of a dual expander of claim 1 wherein said multi-core expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.

14. (new) The method of controlling operation of said dual expander having said first expander core and said second expander core of claim 2 wherein said dual expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.

15. (new) The process for performing said register write operation in said first expander core of said dual expander of claim 3 wherein said dual expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.

16. (new) The process for performing said register write operation in said second expander core of said dual expander of claim 4 wherein said dual expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.

17. (new) The process for performing said register read operation from said first expander core of said dual expander of claim 5 wherein said dual expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.

18. (new) The process for performing said register read operation from said second expander core of said dual expander of claim 6 said dual expander does not require that EPROM contained in said multi-core expander does not need to be removed and reprogrammed.